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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,982	06/24/2003	Jeff Nause	046361/265061	2036

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,982	NAUSE ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, (1) the passivation layer on said gate and said rectifying contacts and on said heterojunction (claim 10); and the dummy gate is formed, and side walls are made on the lateral surface of the dummy gate, and the gate-insulating-film-forming layer is then selectively removed by using the dummy gate and the sidewalls as a mask, thereby forming the gate insulating film (claim 20) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "6" has been used to designate both the gate insulating film and channel layer (page 6, paragraph 17). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 4 is objected to because of the following informalities: there is an unnecessary period punctuation (0.1<x.<.4) in line 3 of said claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 9 thru 11, 14, 16, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "said source and drain contacts" in line 1 of said claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "said gate and said rectifying contacts and on said heterojunction" in line 2 of said claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "the lateral surfaces" in line 1 of said claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitation "ZnO channel" in line 1 of said claim. There is insufficient antecedent basis for this limitation in the claim. It is unclear whether the ZnO channel and a channel layer stated in claim 1 are the same structure.

Claims 16 and 20 recite the limitation "side walls" in line 2 of claim 16 and claim 20. There is insufficient antecedent basis for this limitation in the claim. It is unclear what "side walls" the applicant is referring to.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Insofar as definite, claims 1 thru 9, 11 thru 13, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. 6,469,315 B1 in view of Wolter 4,677,457. Suzuki discloses (see, for example, FIG. 1) a high electron mobility transistor 10 comprising a channel layer 13, gate electrode 21, and barrier layer (gate insulating film) 17. In column 8, lines 3-6, Suzuki discloses the barrier layer comprising $Al_cGa_{1-c}N$ ($0 \leq c \leq 1$) which is a Group-III nitride compound semiconductor. Suzuki does not disclose a channel layer being composed of a II-VI compound semiconductor zinc oxide. However, Wolter discloses (see, for example, FIG. 3a) a high electron mobility transistor comprising charge carrying layers (channel) 1, 2A, 2B. In column 5, lines 16-26, Suzuki discloses the layers comprising gallium arsenide (GaAs) and gallium aluminum arsenide (GaAlAs), however, in column 7, lines 62-column 8, lines 2, Wolter discloses that GaAs and AlGaAs can be replaced by other semiconductor materials such as ZnO (zinc oxide) in order to utilize different band gaps. Therefore it would have been obvious to one of

ordinary skill in the art at the time of invention to have a channel layer being composed of a II-VI compound semiconductor zinc oxide in order to utilize different band gaps in a high electron mobility transistor, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 5, see, for example, column 8, lines 12-15, wherein Suzuki discloses the substrate may be made of sapphire, silicon carbide and the like.

Regarding claim 6, see, for example, column 3, lines 52-53, wherein Suzuki discloses the barrier layer having a thickness, for example, 2 nm (0.30 nanometer (nm) to 50 nm).

Regarding claim 8, see, for example, column 4, lines 1-2, wherein Suzuki discloses the gate electrode being made of gold (Au).

Regarding claim 9, see, for example, FIG. 1 wherein Suzuki discloses source electrode (source contact) 22 and drain electrode (drain contact) 23. In column 4, lines 9-13, Suzuki discloses the source and drain electrode having nickel (Ni) in a layered structure.

Regarding claims 2, 3, 7, 13, 14, and 16, the limitations contain product-by-process language (i.e. epitaxially grown, piezoelectric doping, MOCVD, dummy gate), which does not patentably distinguish the product claims from the prior art.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. 6,469,315 B1 in view of Wolter 4,677,457 as applied to claims 1-9, 11-13, 16, and 17 above, and further in view of Shanfield et al. 5,880,483. Suzuki in view of Wolter does

not disclose a passivation layer on said gate and said rectifying contacts and on said heterojunction. However, Shanfield discloses (see, for example, Fig. 3) a field effect transistor comprising a passivation layer 36 over a gate electrode 24 and source and electrodes 22, 20. The passivation protects the top of the field effect transistor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a passivation layer on said gate and said rectifying contacts and on said heterojunction in order to protect the top of the transistor.

9. Claims 14, 15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. 6,469,315 B1 in view of Wolter 4,677,457 as applied to claims 1-9, 11-13, 16, and 17 above, and further in view of Nishikawa et al. 6,323,053 B1. Suzuki in view of Wolter does not disclose a ZnO substrate and the ZnO substrate being a c-surface substrate. However, Nishikawa discloses (see, for example, column 11, lines 50-55) a semiconductor device comprising a substrate made of ZnO and further discloses that a C surface can be used. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a ZnO substrate and the ZnO substrate being a c-surface substrate in order to form a semiconductor device thereon, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. 6,469,315 B1 in view of Wolter 4,677,457 as applied to claims 1-9, 11-13, 16, and 17

above, and further in view of Ando 6,429,467 B1. Suzuki in view of Wolter does not disclose the gate insulating film being formed by metal organic chemical vapor deposition (MOCVD). However, Ando discloses (see, for example, column 4, lines 43-60) a field effect transistor comprising a gate insulating layer 13 wherein the gate insulating layer is formed by MOCVD. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate insulating film being formed by metal organic chemical vapor deposition (MOCVD) in order to adequately form the gate insulating film in a transistor.

11. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. 6,469,315 B1 in view of Wolter 4,677,457 as applied to claims 1-9, 11-13, 16, and 17 above, and further in view of Kawai et al. 5,929,467. Suzuki in view of Wolter does not disclose a dummy gate being formed, and side walls are made on the lateral surface of the dummy gate, and the gate-insulating-film-forming layer is then selectively removed by using the dummy gate and the sidewalls as a mask. However, Kawai discloses (see, for example, column 2, lines 34-50) a field effect transistor formed by the method of forming a dummy gate; forming side walls on lateral surfaces of the dummy gate; and forming the gate insulating film by selectively removing the gate-insulating-film forming layer using the dummy gate and the side walls as a mask. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a dummy gate being formed, and side walls are made on the lateral surface of the dummy gate, and the gate-insulating-film-forming layer is then selectively removed by using the dummy gate and the sidewalls as a mask in order to adequately form a gate insulating film in a transistor.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
August 1, 2004